UDA.022



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

e U.S. Patent No. 7,098,729 B2

Osamu ABE

Serial No.:

10/647,468

Group Art Unit:

2816

Filing Date:

August 26, 2003

Examiner:

Englund, Terry Lee

For:

BAND GAP CIRCUIT

Honorable Commissioner of Patents Alexandria, Virginia 22313-1450 Certificate

OCT 1 8 2006

of Correction

REQUEST FOR CERTIFICATE OF CORRECTION

Sir:

The undersigned respectfully requests a Certificate of Correction for the above-identified patent. In particular, it is requested that a typographical error in the Assignees's name be corrected to:

NEC Electronics Corporation

Since this error is believed due to the Patent and Trademark Office, no fee is submitted herewith.

Please forward a certificate of Correction to the address shown below. If there are any questions on this matter, please direct all telephone calls to the number shown below.

The Commissioner is authorized charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481

Respectfully submitted,

Sean M. McGinn

Registration No. 34,386

Date:

McGinn Intellectual Property

Law Group, PLLC

8321 Old Courthouse Road, Suite 200

Vienna, Virginia 22182-3817

(703) 761-4100

Customer No. 21254

OCT 18 2006

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.: 7,098,729 B2

DATED : August 29, 2006

INVENTOR(S): Osamu ABE

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

It has been requested that the assignee name be corrected to NEC Electronics Corporation.

(73) Assignee: NEC Electronics Corporation,

Kanagawa (JP)

MAILING ADDRESS OF SENDER (Please do not use customer number

PATENT NO. 7,098,729 B2

No. of additional copies

McGinn Intellectual Property Law Group, PLLC 8321 Old Courthouse Road, Suite 200

Vienna, Virginia 22182-3817

P15/REV03



US007098729B2

(12) United States Patent Abe

US 7,098,729 B2 (10) Patent No.: (45) Date of Patent: Aug. 29, 2006

(54)	BAND GAP CIRCUIT			
(75)	Inventor:	Osamu Abe. Kanagawa (JP)		
(73)	Assignee:	NEC <u>Electronics</u> Corporation. Kanagawa (JP) Electronics		
(*)	Notice:	Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.		
(21)	Appl. No.: 10/647,468			
(22)	Filed:	Aug. 26, 2003		
(65)		Prior Publication Data		
	US 2004/0	051581 A1 Mar. 18, 2004		
(30)	Foreign Application Priority Data			
Aug. 28, 2002 (JP) 2002-249352				
(51)	Int. Cl. G05F 1/575 (2006.01) G05F 1/46 (2006.01)			
(52)	U.S. Cl			
	Field of Classification Search			
(30)	ricid of C	323/313		
	See applica	ation file for complete search history.		
(56)	References Cited			
	U.S	S. PATENT DOCUMENTS		

7/1990 Guo et al. 327/542

7/1993 Kraus et al. 323/313

1/1994 Rundel 327/344

1/2000 Oda 327/546

2/2000 Sharpe-Gelder 323/313

8/2001 Vu 327/539

11/2000 McNeill et al. 327/539

Koifman et al. 327/198

Tokuda 323/313

4.943,737 A *

5,229.710 A *

4/1999

11/1999

5,281,866 A

5,892,381 A

6,031,365 A

6,278,320 B1

5,994,887 A *

6,011,429 A *

6,150,872 A *

6.294,902 B1 *	9/2001	Moreland et al 323/268
6,377,085 B1 *	4/2002	Giuroiu 327/66
6,501,299 B1 *	12/2002	Kim et al 326/83
6,657,480 B1 *	12/2003	Ochi 327/539
6,737,908 B1 *	5/2004	Mottola et al 327/539

FOREIGN PATENT DOCUMENTS

2002-123325 4/2002 TW 210414 8/1993

OTHER PUBLICATIONS

Hitoshi Tanaka, et al., "A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative World-Line Scheme". IEEE Journal of Solid-State Circuites, vol. 34 No. 8, Aug. 1999, pp.

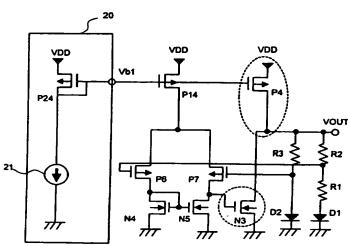
European Search Report dated Aug. 10, 2004. Taiwan Office Action dated Apr. 8, 2005 (with English translation).

* cited by examiner

Primary Examiner—Terry D. Cunningham Assistant Examiner—Terry L. Englund (74) Attorney, Agent, or Firm-McGinn IP Law Group, **PLLC**

ABSTRACT

A band gap circuit, including a differential amplifier. In response to fluctuation of the voltage on the band gap circuit output terminal VOUT, a potential difference occurs at an inverting input terminal and a noninverting input terminal of the differential amplifier. A transistor, connected to the output terminal VOUT, ground, an output terminal of the differential amplifier, causes excess current from the output terminal VOUT to flow to ground in response to fluctuation of the potential at the output terminal of the differential amplifier. A transistor that has a resistive component and a resistor that has a capacitive component are connected between a power supply voltage VDD and the output terminal VOUT.



16 Claims, 8 Drawing Sheets